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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,452	07/23/2003	Kwang-Ok Koh	5649-1144	7953

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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,452	KOH ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/625,452.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *070904*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Ling et al (US 6,153,455)

Ling discloses a method for fabricating a CMOS. The method comprises the steps of:

forming a gate pattern that includes a gate electrode on a substrate (col 4, lines 19-21)

forming lightly doped impurity diffusion layers in the substrate at both sides of the gate pattern (col 4, lines 53-55)

forming spacers on sidewalls of the gate pattern, the spaçer having a bottom width (fig. 1)

implanting impurity ions using the gate pattern and the spaçer as a mask to form a heavily doped impurity diffusion layer in the substrate (col 4, lines 63-65; fig. 1)

removing the spacers (fig. 2)

forming a conformal etch stop layer 113 on the gate pattern and the substrate , wherein the etch stop layer is formed to a thickness of at least the bottom width of the spacer (col 6, lines 1-2; fig. 2)

forming a çonformal etch shield layer on the gate pattern and the substrate , wherein the etch shield layer is formed of insulation material having etch selectivity with respect to the spacers; and wherein the step of forming spacer çomprises forming spacers on the etch shield layer of the sidewall gate pattern.

Regarding claim 5, Ling discloses forming lightly doped drain region (col 4, lines 44-45)

Regarding claim 6, fig. 2 of Ling shows that the layer 113/etch stop layer having a same thickness with the bottom width of spacers on the sidewalls

3. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Pradeep et al (US 6,451,704)

Pradeep discloses a method for fabricating a PLDD structure. The method comprises the steps of:

forming a gate pattern that includes a gate electrode on a substrate (col 6, lines 20-25)

forming lightly doped impurity diffusion layers in the substrate at both sides of the gate pattern (col 8, lines 17-19)

forming spacers 24 on sidewalls of the gate pattern, the spaçer having a bottom width (col 7, lines 65-67; fig. 2)

implanting impurity ions using the gate pattern and the spaçer as a mask to form a heavily doped impurity diffusion layer in the substrate (col 8, lines 25-27; fig. 2)

removing the spacers (col 8, lines 43-44)

forming a conformal etch stop layer 32 on the gate pattern and the substrate , wherein the etch stop layer is formed to a thickness of at least the bottom width of the spacer 24 (col 9, lines 17-19; fig. 4)

Regarding claims 2, 4, Pradeep discloses forming a çonformal etch shield layer 21 on the gate pattern and the substrate, wherein the etch shield layer is formed of insulation material (SiN) having etch selectivity with respect to the spacers (oxide) (col 7, lines 17-19); and wherein the step of forming spacer çomprises forming spacers 24 on the etch shield layer of the sidewall gate pattern (fig. 2)

Regarding claim 3, Pradeep discloses forming a buffer insulation layer 20 (col 7, lines 29-30), the layer 21 is formed on the layer 20 (fig. 2)

Regarding claim 5, Pradeep discloses forming lightly doped drain region (col 4, lines 44-45)

Regarding claim 6, fig. 4 of Pradeep shows that the layer 32/etch stop layer having a same thickness with the bottom width of spacers 24

4. Claims 12-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Pradeep et al (US 6,451,704)

Pradeep discloses a method for fabricating a PLDD structure. The method comprises the steps of:

forming a device isolation layer in a substrate to define first and second active regions (fig. 1)

forming a first gate pattern on the first active region and a second gate pattern on the second active region (col 6, lines 20-25), the first gate pattern and second gate pattern include a gate insulation layer 18, a first gate electrode 14, a first hard mask 22 that are stacked (col 6, lines 17-30; fig. 1)

forming lightly doped impurity diffusion layers in the substrate at both sides of the gate pattern (col 8, lines 17-19)

forming spacers 24 on sidewalls of the first and second gate patterns, the spaçer having a bottom width (col 7, lines 65-67; fig. 2)

implanting impurity ions using the gate pattern and the spaçer as a mask to form a heavily doped impurity diffusion layer in the first active region (col 8, lines 25-27; fig. 2)

removing the spacers (col 8, lines 43-44)

forming a conformal etch stop layer 32 on the first and second gate patterns and the substrate ,wherein the etch stop layer is formed to a thickness of at least the bottom width of the sidewall spacer 24 (col 9, lines 17-19; fig. 4)

The second gate pattern reaches the first active region as shown in fig. 2

Regarding claims 13, 15, Pradeep discloses forming a conformal etch shield layer 21 on the gate pattern and the substrate, wherein the etch shield layer is formed of insulation material (SiN) having etch selectivity with respect to the spacers (oxide) (col

7, lines 17-19); and wherein the step of forming spacer çomprises forming spacers 24 on the etch shield layer on opposite sidewalls of the gate pattern (fig. 2)

Regarding claim 14, Pradeep discloses forming a buffer insulation layer 20 (col 7, lines 29-30), the layer 21 is formed on the layer 20 (fig. 2)

Regarding claim 16, Pradeep discloses forming lightly doped drain region (col 4, lines 44-45)

Regarding claim 17, fig. 4 of Pradeep shows that the layer 32/etch stop layer having a same thickness with the bottom width of spacers 24

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 7-11, 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pradeep et al (US 6,451,704) in view of Tottori (US 6,207,987)

Pradeep method has been described above. Unlike the instant claimed inventions as per claims 7-11, 18-21 Pradeep fails to disclose the steps of forming an interlayer insulating layer (silicon oxide) on the etçh stop layer, patterning the interlayer insulation layer and the etch stop layer to form a contact hole by anisotropically etching to expose the heavily doped impurity diffusion layer and forming a conductive pattern that fill the contact hole

Tottori discloses a method for forming a semiconductor device comprises the steps of forming an interlayer insulating layer (silicon oxide) 9 on the etçh stop layer, patterning the interlayer insulation layer and the etch stop layer to form a contact hole 15b by RIE/anisotropically etching to expose the heavily doped impurity diffusion layer and forming a conductive pattern that fill the contact hole (col 11, lines 1-5, lines 36-40; fig. 8-9)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Pradeep method by adding the steps of forming an interlayer insulating layer (silicon oxide) on the etch stop layer, patterning the interlayer insulation layer and the etch stop layer to form a contact hole by anisotropically etching to expose the heavily doped impurity diffusion layer and forming a conductive pattern that fill the contact hole to form the plug for filling the contact hole and to complete the semiconductor device as taught by Tottori (col 13, lines 20-24)

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
April 25, 2005